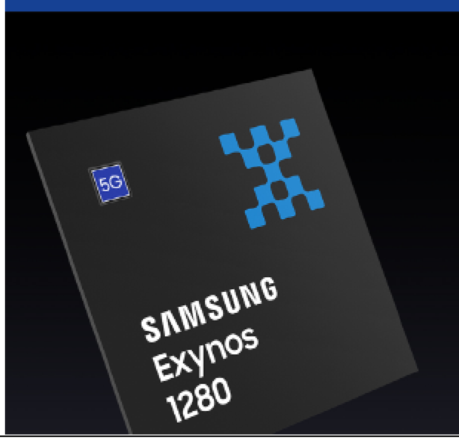
EXHIBIT 021

'052 Patent Claim	Samsung Exynos 1280 System on Chip[1]
6. Method of communication service mapping in an integrated circuit, having a plurality of processing modules (M, S),	Without conceding that the preamble of claim 6 of the '052 Patent is limiting, Samsung Electronics Co., Ltd.'s (hereinafter, "Samsung") Exynos 1280 system on chip (hereinafter, the "Exynos SoC") is an integrated circuit and performs a method of communication service mapping in an integrated circuit, having a plurality of processing modules (M, S), either literally or under the doctrine of equivalents.

[1] The Exynos SoC is charted as a representative product made used, sold, offered for sale, and/or imported by or on behalf of Samsung. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein.

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	SAMSUNG **Product brief** Create infinite possibilities **Exynos 1280** **Highlights** A mobile processor ready for 5G and AI Advanced ISP and MFC for rich multimedia experience Powerful octa-core CPU and GPU  **5G for all** Exynos 1280 is a mobile processor based on a 64-bit RISC processor. It contains a 5G modem, which is compliant with two types of 5G network (Sub-6GHz and mmWave), as well as all legacy networks. It is built using an advanced 5nm EUV process for high power efficiency. **All-in-one processor for 5G** The Exynos 1280 embedded modem supports both sub-6GHz (Frequency Range

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U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	https://semiconductor.samsung.com/resources/brochure/Exynos1280.pdf The Exynos SoC comprises a plurality of processing modules (M, S), for example Arm Cortex-A78 core, Cortex-A55 core, Arm Mali-G68 GPU, and AI Engine with NPU: **Specifications** (see table below) https://semiconductor.samsung.com/resources/brochure/Exynos1280.pdf

Specifications

	Exynos 1280
CPU	Cortex®-A78 x 2 + Cortex®-A55 x 6
GPU	Mali™-G68
AI	AI Engine with NPU
Modem	5G NR Sub-6GHz 2.55Gbps (DL) / 1.28Gbps (UL) 5G NR mmWave 1.84Gbps (DL) / 0.92Gbps (UL) LTE Cat.18 6CC 1.2Gbps (DL) / Cat.18 2CC 200Mbps (UL)
Connectivity	WiFi 802.11ac MIMO with Dual-band (2.4/5G), Bluetooth® 5.2, FM Radio Rx
GNSS	Quad-constellation multi-signal for L1 and L5 GNSS
Camera	Up to 108MP in single camera mode, Single-camera 32MP @30fps
Video	4K 30fps encoding and decoding
Display	Full HD+@120Hz
Memory	LPDDR4x
Storage	UFS v2.2
Process	5nm

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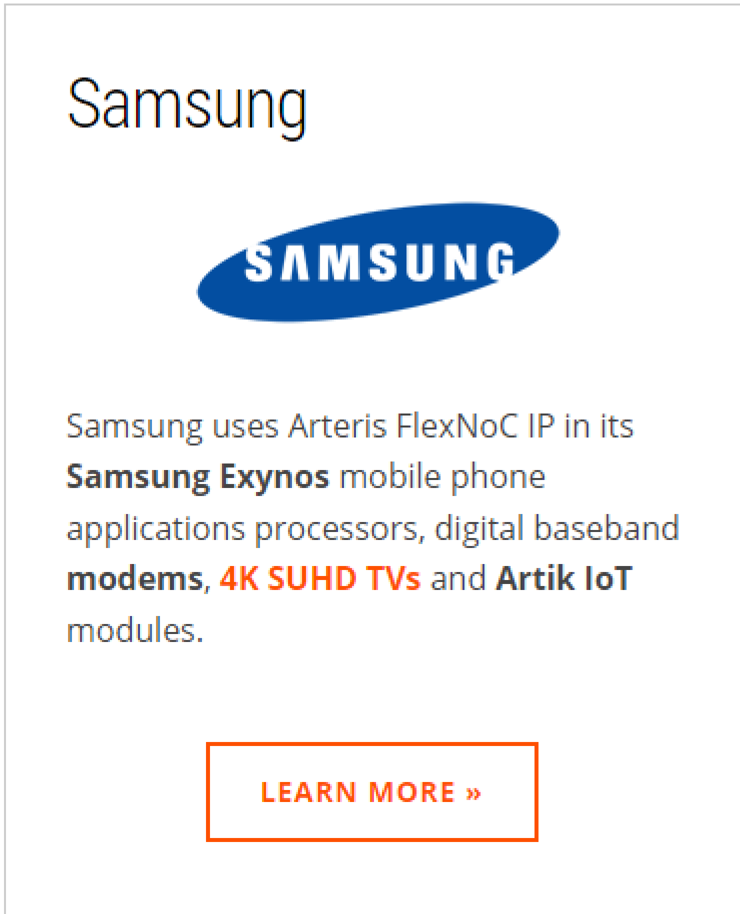
'052 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	The Exynos SoC utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the "Arteris NoC") for communication service mapping:



https://web.archive.org/web/20210514110614/https://www.arteris.com/customers

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'052 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	Arteris IP FlexNoC® Interconnect Licensed by Samsung's System LSI Business for Digital TV Chips by **Kurt Shuler**, on April 23, 2019 CAMPBELL, Calif. –April 23, 2019– Arteris IP, the world's leading supplier of innovative, silicon-proven network-on-chip (NoC) interconnect semiconductor intellectual property, today announced that Samsung's System LSI Business has renewed multiple Arteris IP FlexNoC Interconnect licenses for use in multiple high-performance digital TV (DTV) processing chips utilizing Samsung's latest semiconductor technology process nodes. *Over many years, FlexNoC interconnect IP has helped us accelerate implementation of our digital TV chip designs on our latest semiconductor process nodes. This core interconnect technology is required to develop complex and highly optimized chips in a predictable, low-risk fashion."* SAMSUNG *Jaeyoul Lee, Vice President, **Samsung Electronics*** Samsung first licensed FlexNoC interconnect IP in 2010. Since then, Samsung has used Arteris interconnect IP to enable complex SoC architectures in chips like the Exynos mobile processors and other electronic systems. https://www.arteris.com/press-releases/samsung-lsi-dtv-arteris-ip-flexnoc

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'052 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	Arteris Interconnect IP Solution Selected by Samsung for Mobile SoC Deployment by **Kurt Shuler**, on November 02, 2010 Network-on-Chip (NoC) interconnect technology leader enables higher performance and more cost effective designs for mobile phone systems-on-chip (SoCs) SUNNYVALE, California — November 2, 2010 — Arteris, Inc., a leading supplier of on-chip interconnect IP solutions, today announced that Samsung Electronics Co., Ltd., has selected Arteris' interconnect solutions for multiple chips within Samsung's mobile SOC products. Samsung chose Arteris interconnect IP to support the high speed inter-chip communication requirements in next generation mobile SOC products. *The Arteris interconnect IP offers us a convenient solution to handle the high speed communication needed between our SoC and external modem IC. Our customers will benefit from the lower BOM cost and power consumption as a result of this IP. We look forward to Arteris' interconnect IP helping us shorten development schedules and lower risks associated with compatibility.* SAMSUNG *Thomas Kim, Vice President, SoC Platform Development, System LSI, **Samsung Electronics*** https://www.arteris.com/press-releases/pr_2010_nov_02?hsLang=en-us

'052 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	The Arteris NoC performs communication service mapping in the Exynos SoC. For example, the Arteris NoC uses Network Interface Units (NIUs), which "translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols" and in the Arteris NoC "[m]ost transactions require the following two-step transfers," including "[a] master send[ing] request packets" and "the slave return[ing] response packets": ***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets

'052 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

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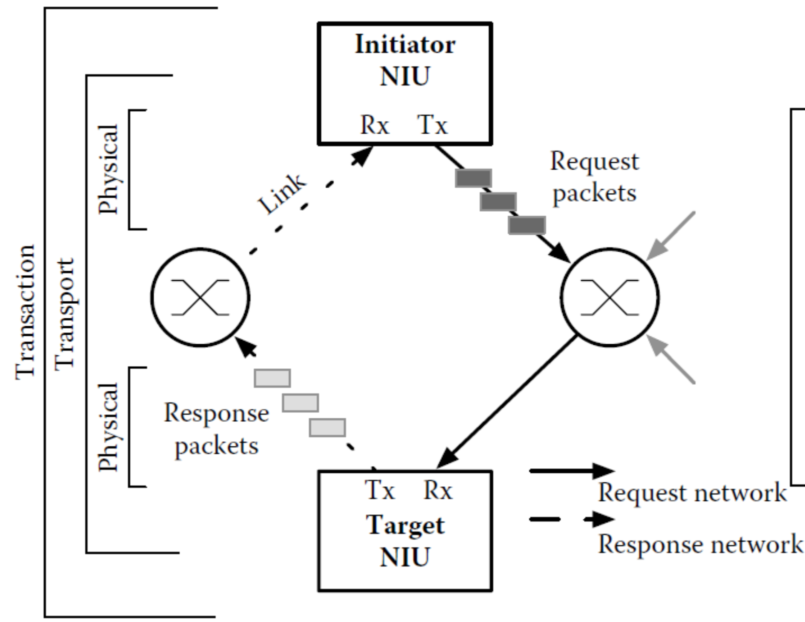
<table>
<tr><th>'052 Patent Claim</th><th>Samsung Exynos 1280 System on Chip[1]</th></tr>
<tr><td></td><td>


FIGURE 11.1
NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.

See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313; *see id* at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: "In this chapter we will present an MPSoC platform […] using Arteris NoC as communication infrastructure.").
</td></tr>
<tr><td>wherein at least one first of said processing modules (M) requests at least</td><td>Without conceding that the preamble of claim 6 of the '052 Patent is limiting, at least one first of said processing modules (M) of the Exynos SoC utilizes the Arteris NoC to request at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification wherein said at least one communication service identification comprises at least one communication thread or at</td></tr>
</table>

'052 Patent Claim	Samsung Exynos 1280 System on Chip[1]
one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region	least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S), either literally or under the doctrine of equivalents. For example, the Arteris NoC utilized by the Exynos SoC uses Network Interface Units (NIUs), which "translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols" and in the Arteris NoC, "[m]ost transactions require the following two-step transfers," including "[a] master send[ing] request packets" and "the slave return[ing] response packets": ***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets

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within said one or more second processing modules (S),	on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

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	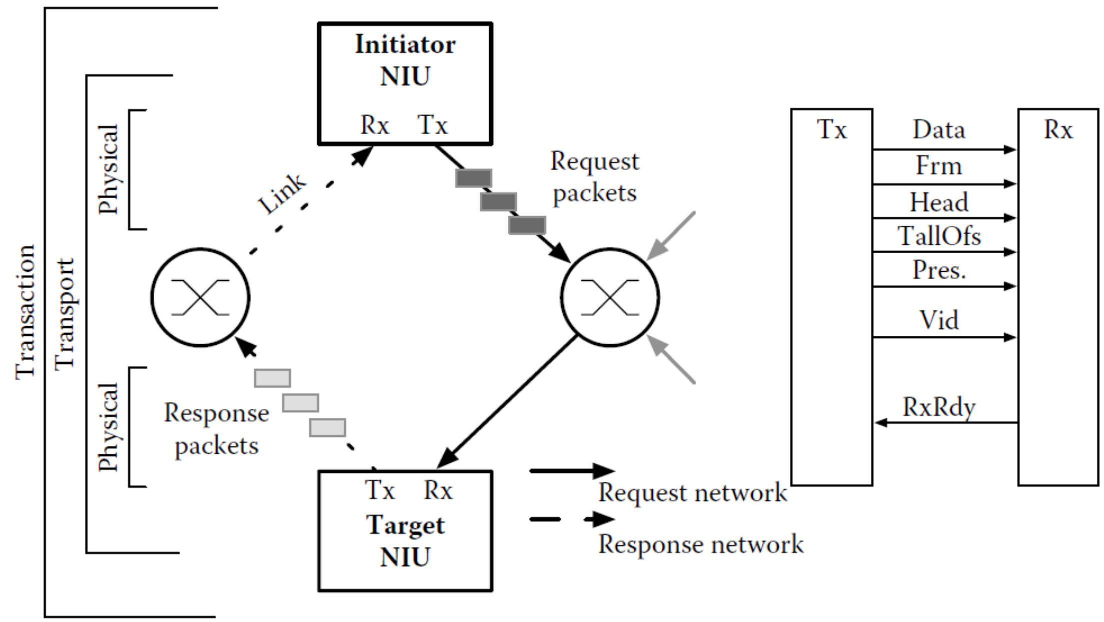 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313. The "Arteris NTTP protocol is packet-based" and the packets, which have "header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address," are "transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes":

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	11.3.1.2 Transport Layer The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target. *Id.* at 313. As yet a further illustration, packets in the Arteris NoC are "delivered as words that are sent along links and "[o]ne link (represented in Figure 11.1) defines the following signals," which include "the current priority of the packet used to define preferred traffic class (or Quality of Service)" and "[f]low control":

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	maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals: • **Data**—Data word of the width specified at design-time. • **Frm**—When asserted high, indicates that a packet is being transmitted. • **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only. • **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only. • **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2). • **Vld**—Data valid: when asserted high, indicates that a word is being transmitted. • **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

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<tr><th>'052 Patent Claim</th><th>Samsung Exynos 1280 System on Chip[1]</th></tr>
<tr><td></td><td>
Id. at 313-314.
As a further example, the packets sent in the Arteris NoC are "composed of cells that are organized into fields, with each field carrying specific information," including "Pres," "Slave address" and "Slave offset":
<table>
<tr><th>Field</th><th>Size</th><th>Function</th></tr>
<tr><td>Opcode</td><td>4 bits/3 bits</td><td>Packet type: 4 bits for requests, 3 bits for responses</td></tr>
<tr><td>MstAddr</td><td>User Defined</td><td>Master address</td></tr>
<tr><td>SlvAddr</td><td>User Defined</td><td>Slave address</td></tr>
<tr><td>SlvOfs</td><td>User Defined</td><td>Slave offset</td></tr>
<tr><td>Len</td><td>User Defined</td><td>Payload length</td></tr>
<tr><td>Tag</td><td>User Defined</td><td>Tag</td></tr>
<tr><td>Prs</td><td>User defined (0 to 2)</td><td>Pressure</td></tr>
<tr><td>BE</td><td>0 or 4 bits</td><td>Byte enables</td></tr>
<tr><td>CE</td><td>1 bit</td><td>Cell error</td></tr>
<tr><td>Data</td><td>32 bits</td><td>Packet payload</td></tr>
<tr><td>Info</td><td>User Defined</td><td>Information about services supported by the NoC</td></tr>
<tr><td>Err</td><td>1 bit</td><td>Error bit</td></tr>
</table>
</td></tr>
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StartOfs	2 bits	Start offset
StopOfs	2 bits	Stop offset
WrpSize	4 bits	Wrap size
Rsv	Variable	Reserved
CtlId	4 bits/3 bits	Control identifier, for control packets only
CtlInfo	Variable	Control information, for control packets only
EvtId	User defined	Event identifier, for event packets only

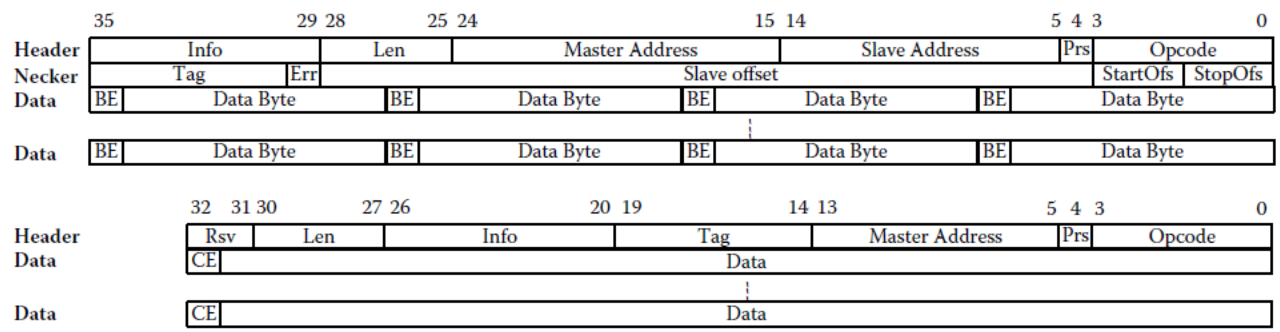

FIGURE 11.2
NTTP packet structure.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 314-315.

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	As further illustration, "[f]or the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2)." *Id.* at 318.
comprising the steps of: coupling said plurality of processing modules (M, S) by an interconnect means (N) and enabling a connection based communication having a set of connection properties,	The Arteris NoC utilized by the Exynos SoC couples the plurality of processing modules (M, S) by an interconnect means (N) and enables a connection based communication having a set of connection properties, either literally or under the doctrine of equivalents. The Arteris NoC couples the plurality of processing modules in the Exynos SoC by an interconnect means. A large SoC, such as the Exynos SoC may include multiple classes of Arteris NoC interconnect:

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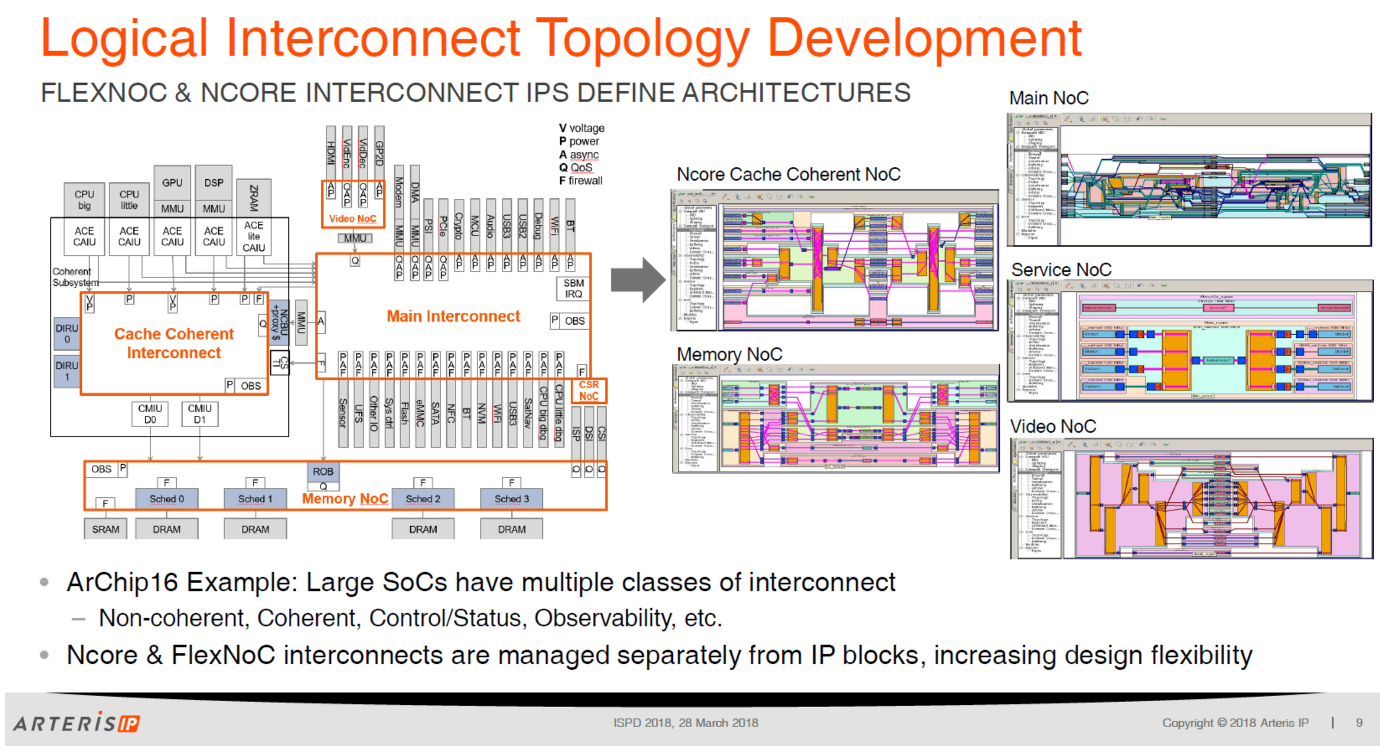

See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.

The Arteris NoC enables a connection based communication having a set of connection properties.

For example, in the Arteris NoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.… Transactions are handed off to the transport layer, which is responsible for delivering

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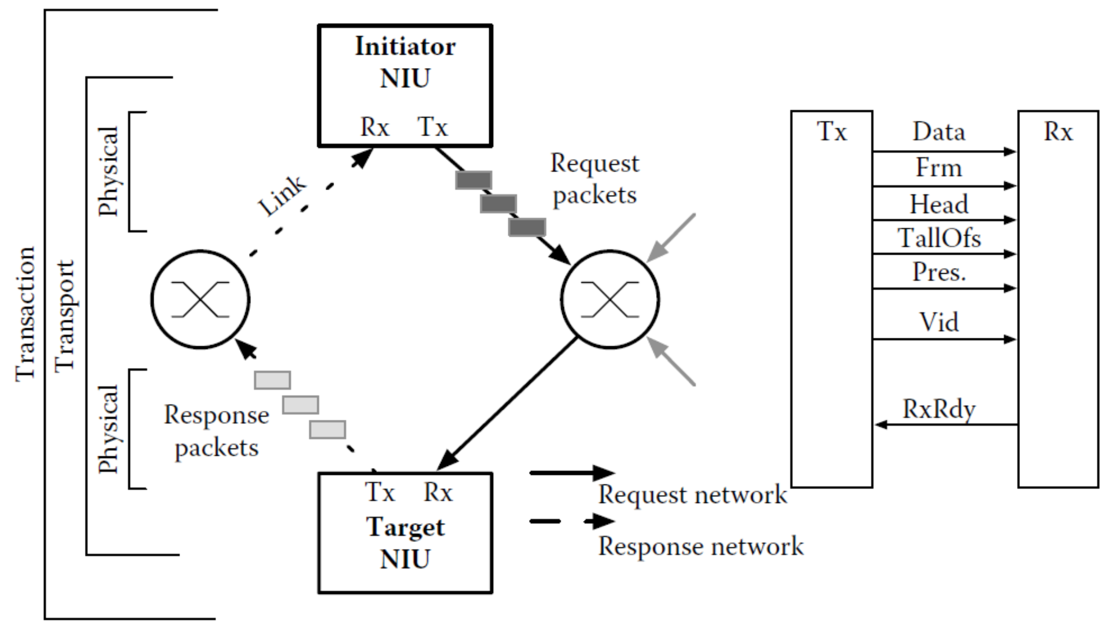
	packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."  **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.

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	The "Arteris NTTP protocol is packet-based" and the packets, which have "header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address," are "transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes": ***11.3.1.2 Transport Layer*** The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target. *Id.* at 313. As a further illustration, packets in the Arteris NoC are "delivered as words that are sent along links and "[o]ne link (represented in Figure 11.1) defines the following signals," which include "the current priority of the packet used to define preferred traffic class (or Quality of Service)" and "[f]low control":

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	maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals: • **Data**—Data word of the width specified at design-time. • **Frm**—When asserted high, indicates that a packet is being transmitted. • **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only. • **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only. • **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2). • **Vld**—Data valid: when asserted high, indicates that a word is being transmitted. • **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

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	Id. at 313-314. As yet a further illustration, the Arteris NoC implements Quality of Service (QoS) to "provide[] a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic"; QoS, which includes guarantees of, for example, throughput and/or latency, "is achieved by exploiting the signal pressure embedded into the NTTP packet definition" where the "pressure signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed"; and the "pressure information will be embedded in the NTTP packet at the NIU level": **Quality of Service (QoS).** The QoS is a very important feature in the interconnect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic. Usually the end users are looking for guarantees on bandwidth and/or end-to-end communication latency. Different mechanisms and strategies have been proposed in the literature. For instance, in Æthereal NoC [11,24] proposed by NXP, a TDMA approach allows the specification of two traffic categories [25]: BE and GT. In the Arteris NoC, the QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition (Figures 11.1 and 11.2). The pressure

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	signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed. For example, we can imagine associating the generation of the pressure signal when a certain threshold has been reached in the FIFO of the corresponding IP. This pressure information will be embedded in the NTTP packet at the NIU level: packets that have pressure bits equal to zero will be considered without QoS; packets with a nonzero value of the pressure bit will indicate preferred traffic class.* Such a QoS mechanism offers immediate service to the most urgent inputs and variables, and fair service whenever there are multiple contending inputs of equal urgency (BE). Within switches, arbitration decisions favor preferred packets and allocate remaining bandwidth (after preferred packets are served) fairly to contending packets. When there are contending preferred packets at the same pressure level, arbitration decisions among them are also fair. The Arteris NoC supports the following four different traffic classes:

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	• **Real time and low latency (RTLL)**—Traffic flows that require the lowest possible latency. Sometimes it is acceptable to have brief intervals of longer latency as long as the average latency is low. Care must be taken to avoid starving other traffic flows as a side effect of pursuing low latency. • **Guaranteed throughput (GT)**—Traffic flows that must maintain their throughput over a relatively long time interval. The actual bandwidth needed can be highly variable even over long intervals. Dynamic pressure is employed for this traffic class. • **Guaranteed bandwidth (GBW)**—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval. Over short periods, the network may lag or lead in providing this bandwidth. Bandwidth meters may be inserted onto links in the NoC to regulate these flows, using either of the two methods. If the flow is assigned high pressure, the meter asserts backpressure (flow control) to prevent the flow from exceeding a maximum bandwidth. Alternatively, the meter can modulate the flows pressure (priority) dynamically as needed to maintain an average bandwidth. • **Best effort (BE)**—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

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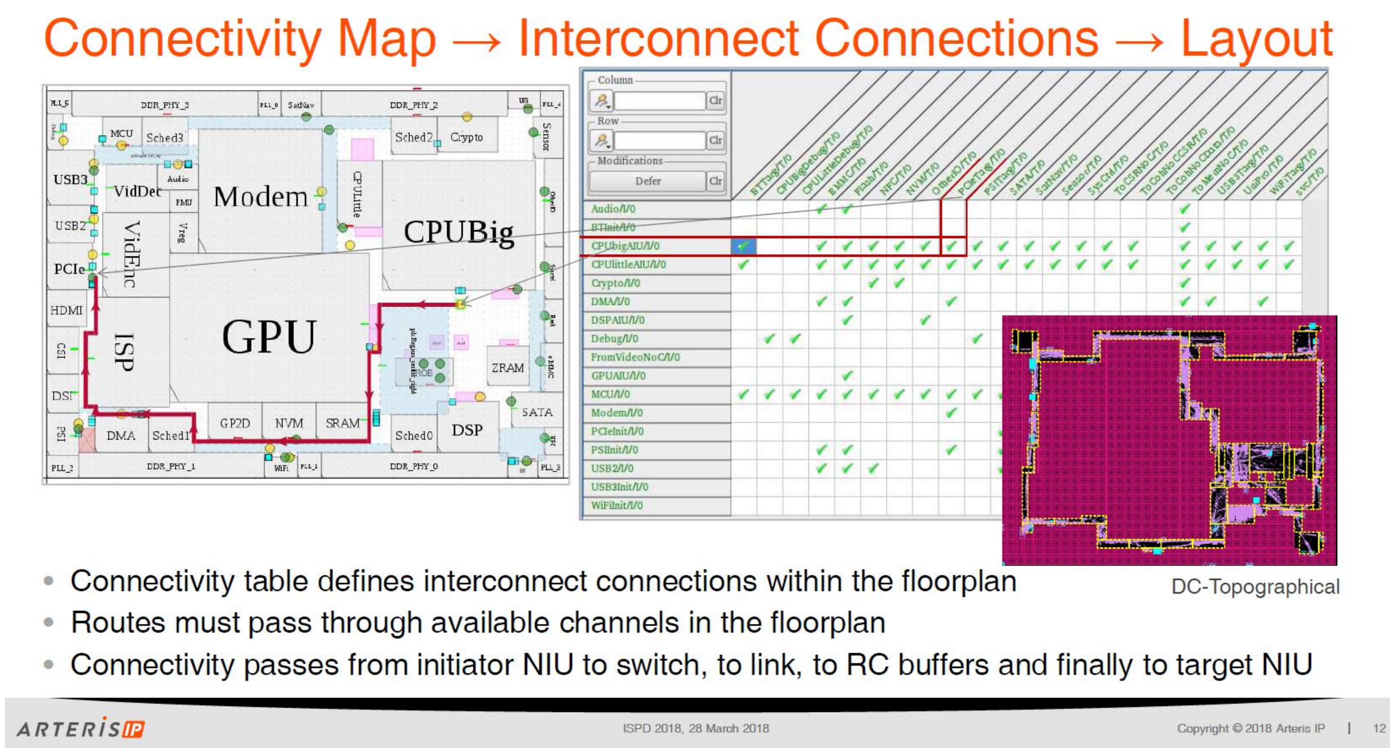
* Note that in the NTTP packet, the pressure field allows more then one bit, resulting in multiple levels of preferred traffic.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 315-316.

Connections within the Arteris NoC interconnect may be defined by a connectivity table:



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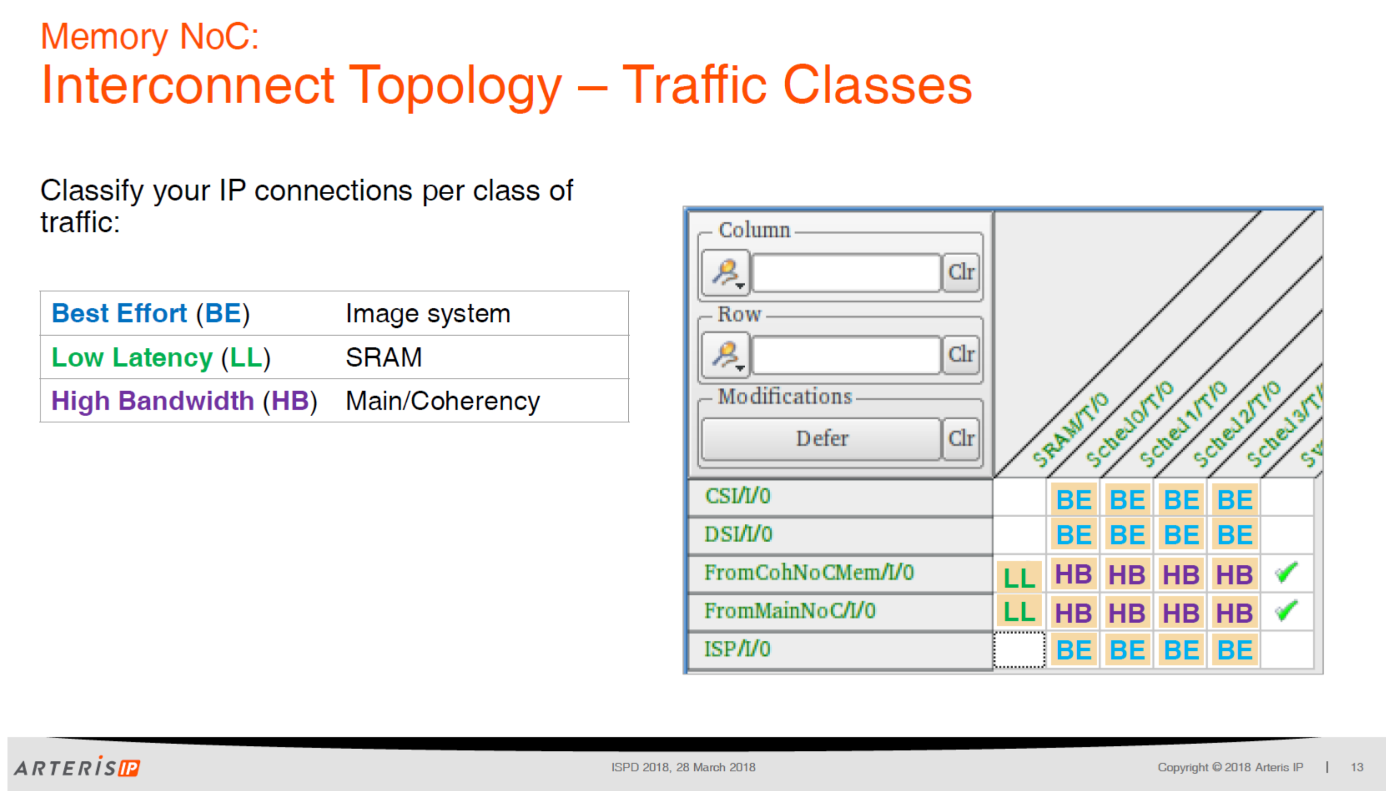
	See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12. As a further illustration, connections within the Arteris NoC may be classified by traffic class and traffic classes, including related to, for example, latency, may be mapped onto the Arteris interconnect topology: 

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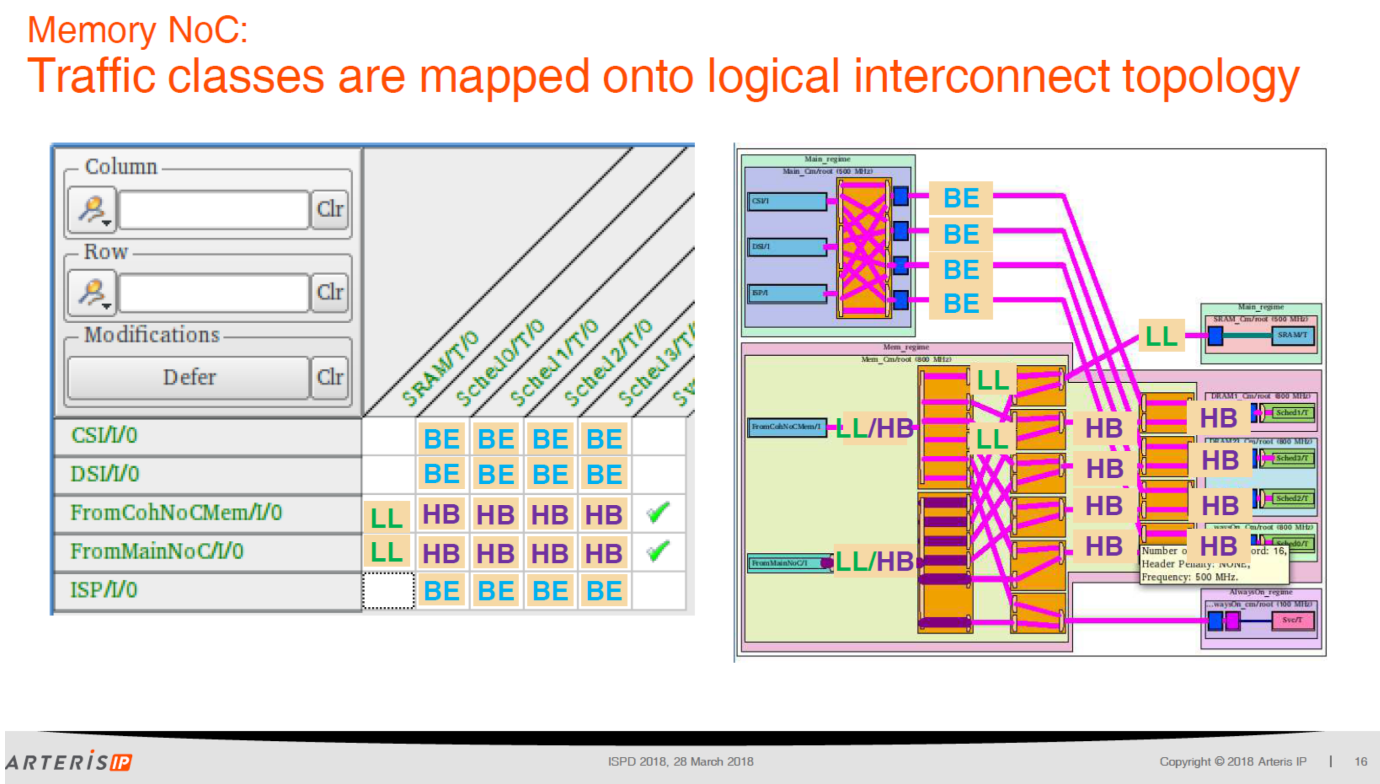
'052 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	

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U.S. Patent No. 7,594,052 (Radulescu & Goossens)
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	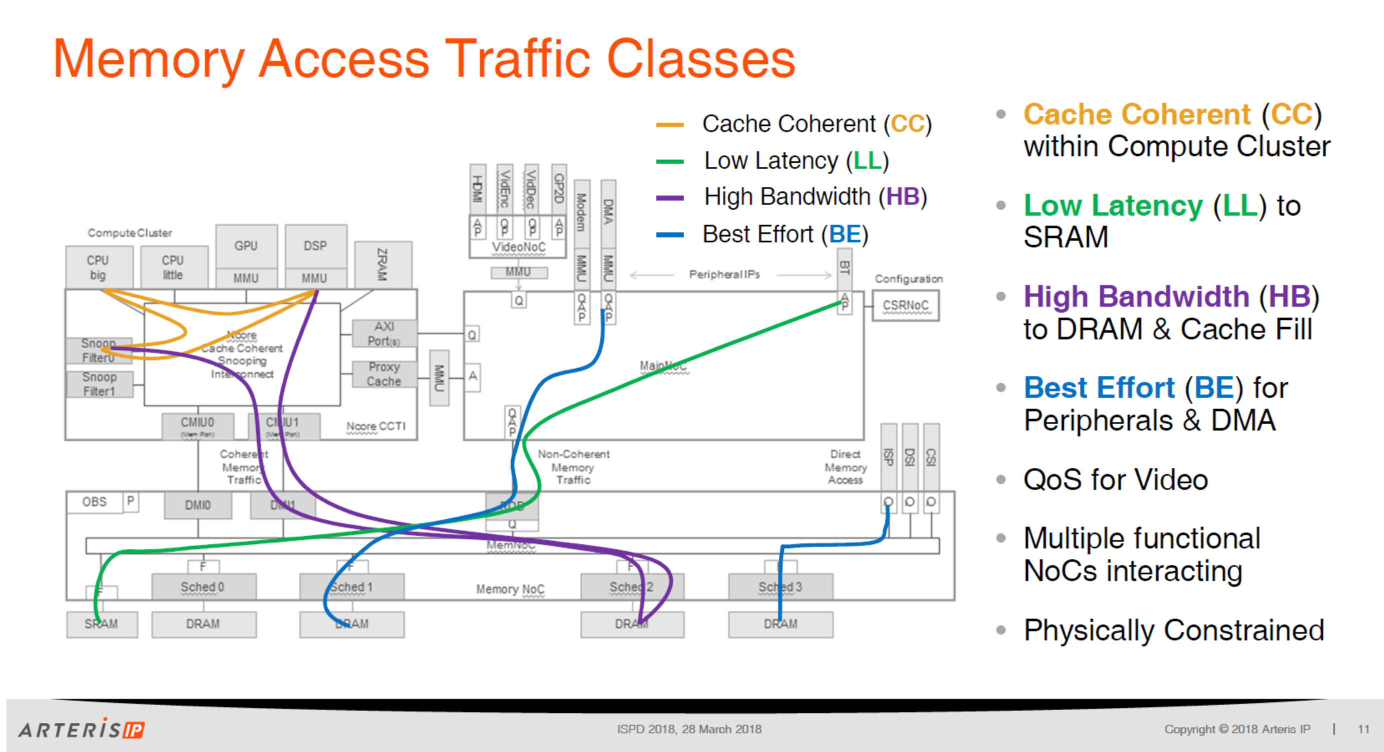 *See* Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slides 11, 13, 16.
controlling the communication between said at least one first of said plurality of	The Arteris NoC utilized by the Exynos SoC controls the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N) by at least one network interface (NI) associated to said at least one first of said processing modules, either literally or under the doctrine of equivalents.

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processing modules (M) and said interconnect means (N) by at least one network interface (NI) associated to said at least one first of said processing modules,	For example, the Arteris NoC used by the Exynos SoC has "Network Interface Units (NIU) connecting IP blocks to the network" with "[i]nterface units for OCP, AMBA AHB, APB, and AXI protocols […] provided." Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311. In the Arteris NoC, "[t]ransaction layer services are provided to the nodes at the periphery of the NoC by special units called Network Interface Units (NIUs)." *Id.* In the Arteris NoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network…. Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."

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	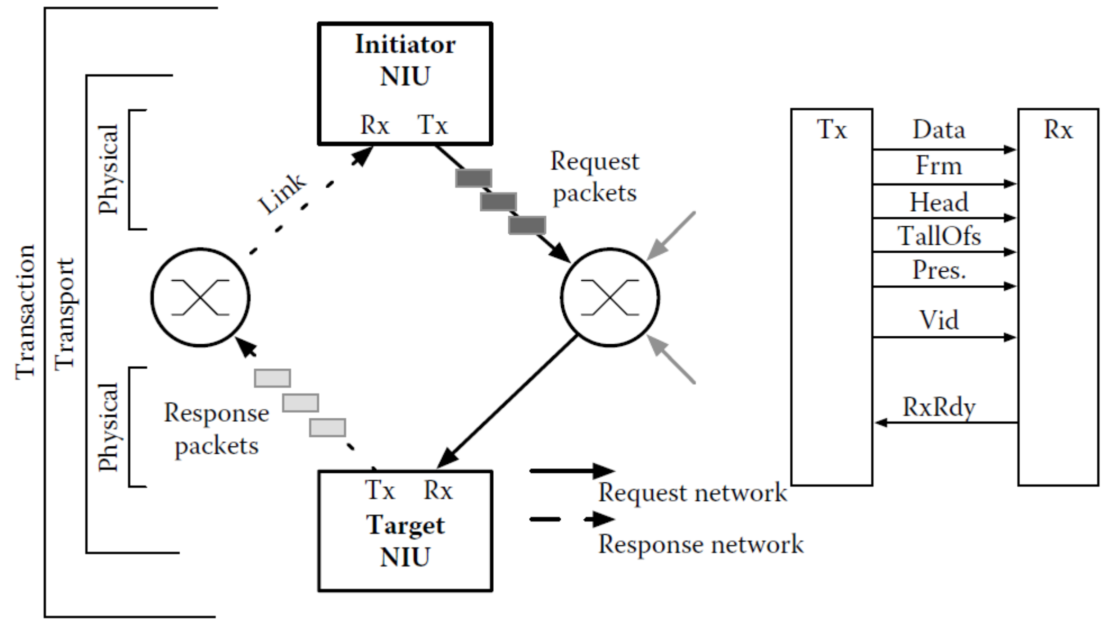 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313. In the Arteris NoC, "transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols":

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	11.3.1.1 Transaction Layer The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network. *Id.* at 312-313.

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mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.	The Arteris NoC utilized by the Exynos SoC maps the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification, either literally or under the doctrine of equivalents. For example, in the Arteris NoC used by the Exynos SoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network…. Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."

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	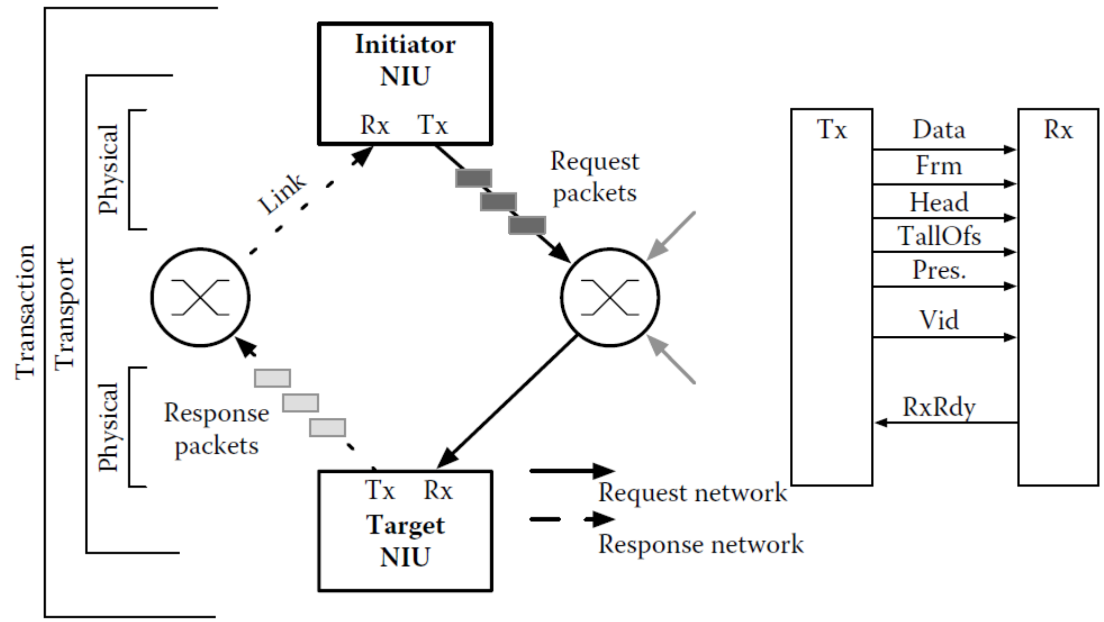 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313. As a further illustration, the "Arteris NTTP protocol is packet-based" and the packets, which have "header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address," are "transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes":

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	11.3.1.2 Transport Layer The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target. *Id.* at 313. As yet a further illustration, packets in the Arteris NoC are "delivered as words that are sent along links and "[o]ne link (represented in Figure 11.1) defines the following signals," which include "the current priority of the packet used to define preferred traffic class (or Quality of Service)" and "[f]low control":

	maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals: • **Data**—Data word of the width specified at design-time. • **Frm**—When asserted high, indicates that a packet is being transmitted. • **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only. • **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only. • **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2). • **Vld**—Data valid: when asserted high, indicates that a word is being transmitted. • **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

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	Id. at 313-314. As a further example, the packets sent in the Arteris NoC are "composed of cells that are organized into fields, with each field carrying specific information," including "Pres," "Slave address" and "Slave offset": <table><tr><th>Field</th><th>Size</th><th>Function</th></tr><tr><td>Opcode</td><td>4 bits/3 bits</td><td>Packet type: 4 bits for requests, 3 bits for responses</td></tr><tr><td>MstAddr</td><td>User Defined</td><td>Master address</td></tr><tr><td>SlvAddr</td><td>User Defined</td><td>Slave address</td></tr><tr><td>SlvOfs</td><td>User Defined</td><td>Slave offset</td></tr><tr><td>Len</td><td>User Defined</td><td>Payload length</td></tr><tr><td>Tag</td><td>User Defined</td><td>Tag</td></tr><tr><td>Prs</td><td>User defined (0 to 2)</td><td>Pressure</td></tr><tr><td>BE</td><td>0 or 4 bits</td><td>Byte enables</td></tr><tr><td>CE</td><td>1 bit</td><td>Cell error</td></tr><tr><td>Data</td><td>32 bits</td><td>Packet payload</td></tr><tr><td>Info</td><td>User Defined</td><td>Information about services supported by the NoC</td></tr><tr><td>Err</td><td>1 bit</td><td>Error bit</td></tr></table>

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StartOfs	2 bits	Start offset
StopOfs	2 bits	Stop offset
WrpSize	4 bits	Wrap size
Rsv	Variable	Reserved
CtlId	4 bits/3 bits	Control identifier, for control packets only
CtlInfo	Variable	Control information, for control packets only
EvtId	User defined	Event identifier, for event packets only

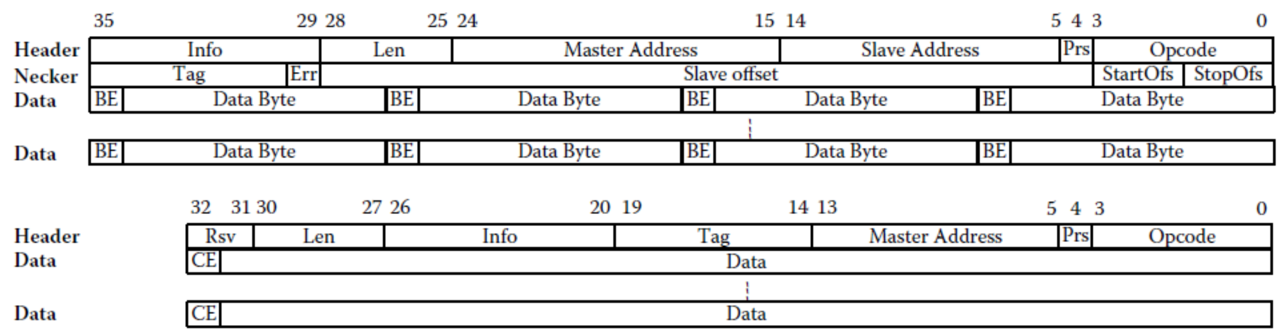

FIGURE 11.2
NTTP packet structure.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 314-315.

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	As further illustration, "[f]or the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2)." *Id.* at 318. As a further illustration, the Arteris NoC implements Quality of Service (QoS) to "provide[] a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic"; QoS, which includes guarantees of, for example, throughput and/or latency, "is achieved by exploiting the signal pressure embedded into the NTTP packet definition" where the "pressure signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed"; and the "pressure information will be embedded in the NTTP packet at the NIU level": **Quality of Service (QoS).** The QoS is a very important feature in the interconnect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic. Usually the end users are looking for guarantees on bandwidth and/or end-to-end communication latency. Different mechanisms and strategies have been proposed in the literature. For instance, in Æthereal NoC [11,24] proposed by NXP, a TDMA approach allows the specification of two traffic categories [25]: BE and GT. In the Arteris NoC, the QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition (Figures 11.1 and 11.2). The pressure

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	signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed. For example, we can imagine associating the generation of the pressure signal when a certain threshold has been reached in the FIFO of the corresponding IP. This pressure information will be embedded in the NTTP packet at the NIU level: packets that have pressure bits equal to zero will be considered without QoS; packets with a nonzero value of the pressure bit will indicate preferred traffic class.* Such a QoS mechanism offers immediate service to the most urgent inputs and variables, and fair service whenever there are multiple contending inputs of equal urgency (BE). Within switches, arbitration decisions favor preferred packets and allocate remaining bandwidth (after preferred packets are served) fairly to contending packets. When there are contending preferred packets at the same pressure level, arbitration decisions among them are also fair. The Arteris NoC supports the following four different traffic classes:

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	• **Real time and low latency (RTLL)**—Traffic flows that require the lowest possible latency. Sometimes it is acceptable to have brief intervals of longer latency as long as the average latency is low. Care must be taken to avoid starving other traffic flows as a side effect of pursuing low latency. • **Guaranteed throughput (GT)**—Traffic flows that must maintain their throughput over a relatively long time interval. The actual bandwidth needed can be highly variable even over long intervals. Dynamic pressure is employed for this traffic class. • **Guaranteed bandwidth (GBW)**—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval. Over short periods, the network may lag or lead in providing this bandwidth. Bandwidth meters may be inserted onto links in the NoC to regulate these flows, using either of the two methods. If the flow is assigned high pressure, the meter asserts backpressure (flow control) to prevent the flow from exceeding a maximum bandwidth. Alternatively, the meter can modulate the flows pressure (priority) dynamically as needed to maintain an average bandwidth. • **Best effort (BE)**—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

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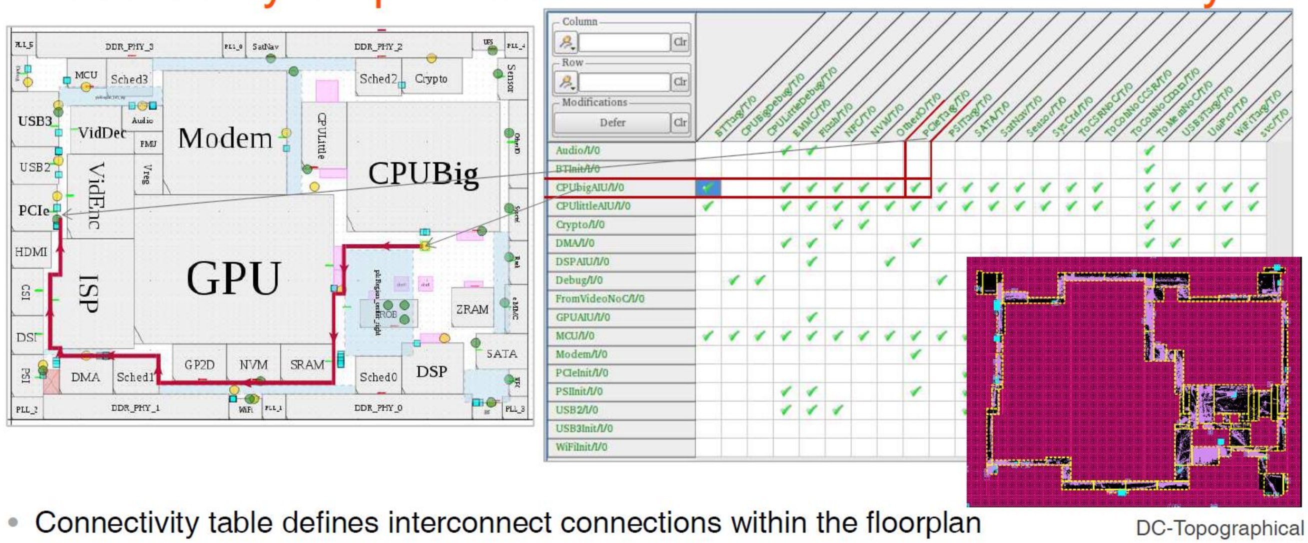
* Note that in the NTTP packet, the pressure field allows more then one bit, resulting in multiple levels of preferred traffic.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 315-316.

Connections within the Arteris NoC interconnect may be defined by a connectivity table:

Connectivity Map → Interconnect Connections → Layout



- Connectivity table defines interconnect connections within the floorplan
- Routes must pass through available channels in the floorplan
- Connectivity passes from initiator NIU to switch, to link, to RC buffers and finally to target NIU

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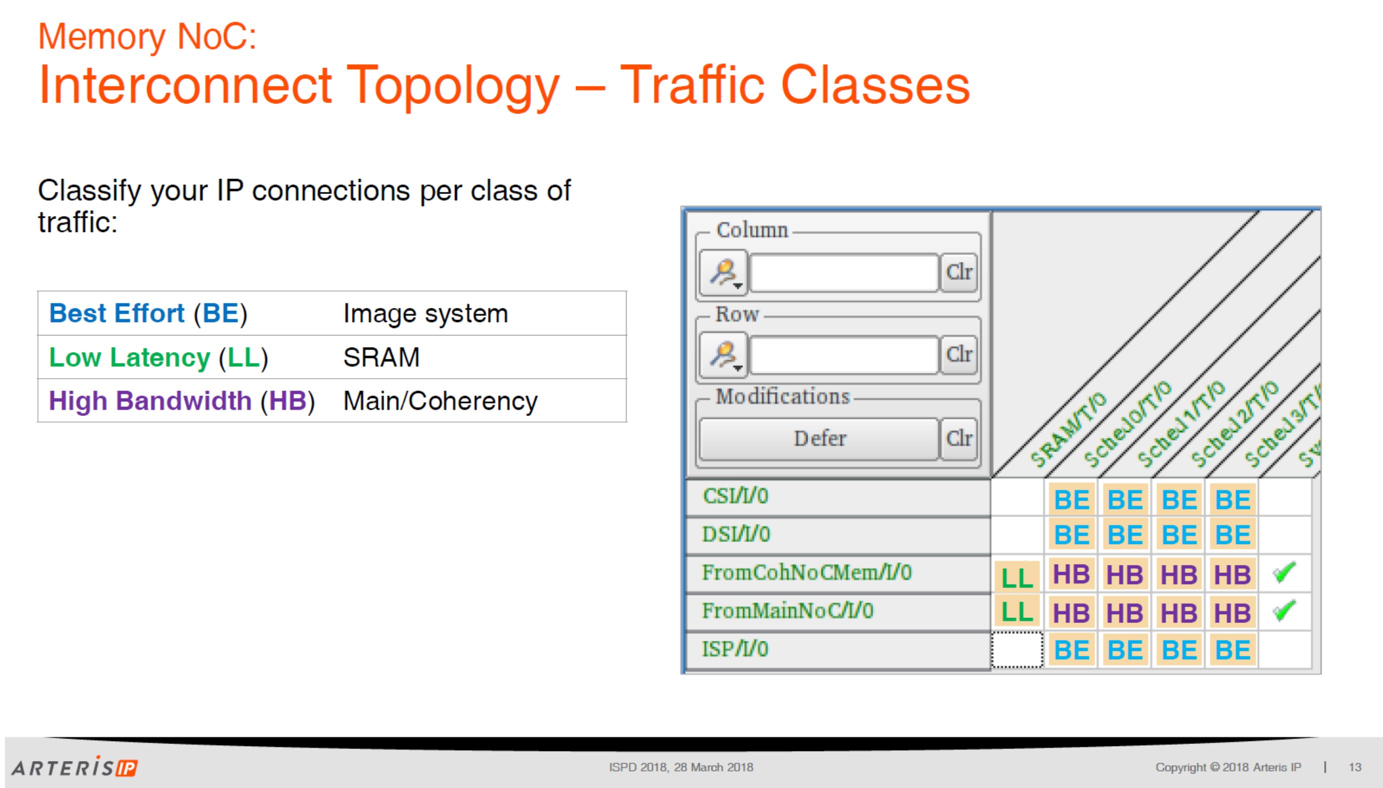
	See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12. As a further illustration, connections within the Arteris NoC may be classified by traffic class and traffic classes, including related to, for example, latency, may be mapped onto the Arteris interconnect topology:



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	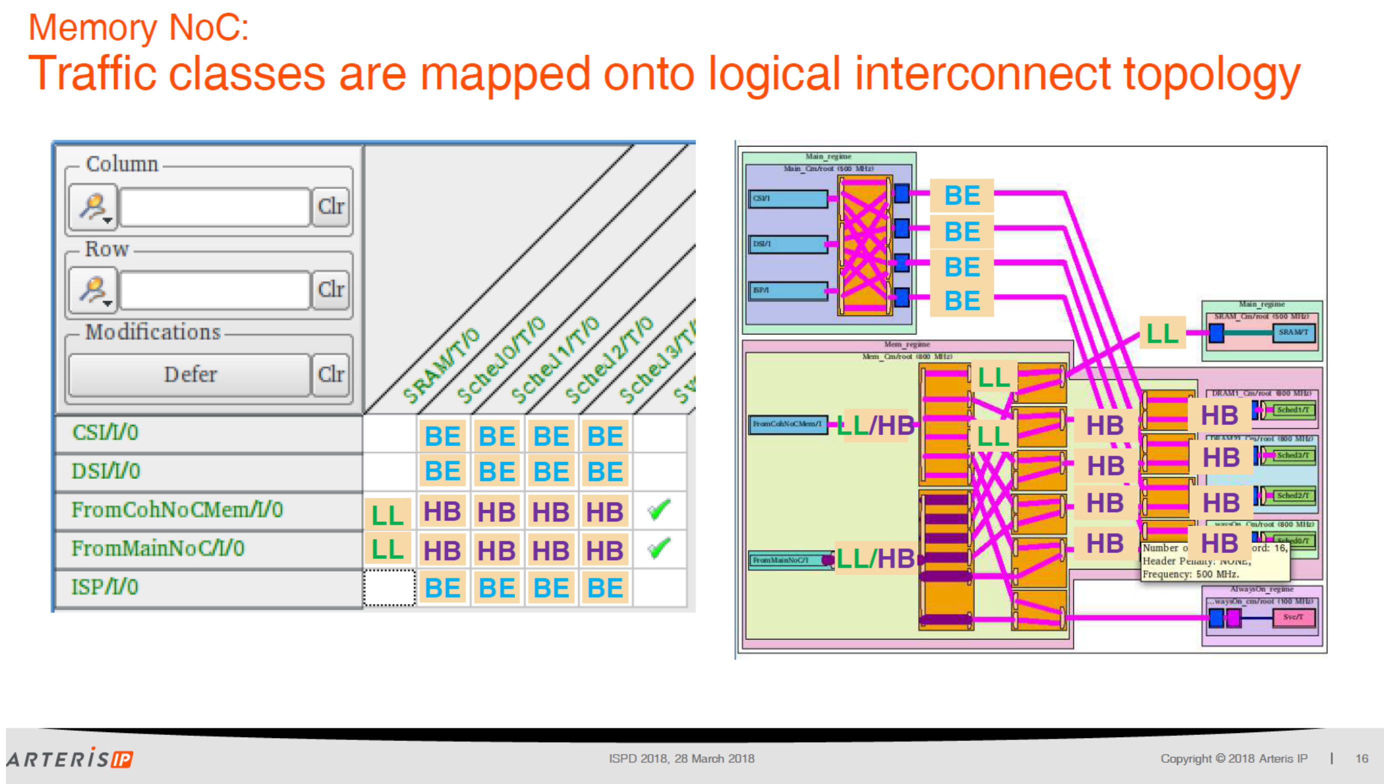

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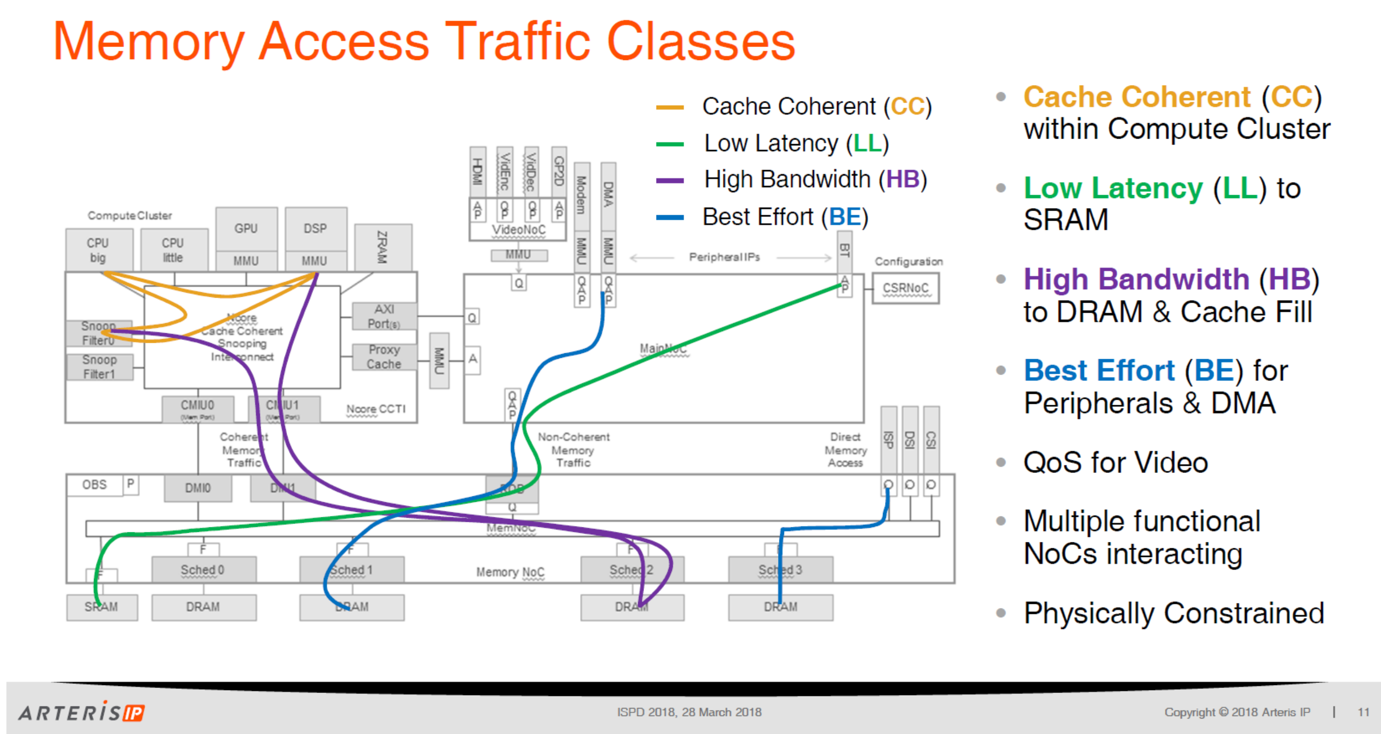

See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slides 11, 13, 16.

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